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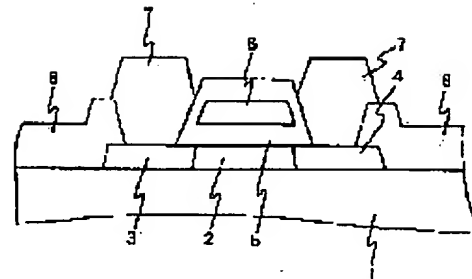
(21)Application number : 10-296401 (71)Applicant : HITACHI LTD
(22)Date of filing : 19.10.1998 (72)Inventor : KOIKE YOSHIHIKO
KO CHIYUUKOU
AOYAMA TAKASHI
OKAJIMA YOSHIAKI

(54) LASER ANNEALING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To obtain a large carrier mobility, by orienting specific surface of a poly-Si layer constituting a TFT which is a semiconductor device formed on an insulating substrate, such as a glass substrate, etc.

SOLUTION: After a surface protective film is deposited on a glass substrate 1 by on atmospheric pressure CVD method while the substrate 1 is maintained at 480° C, poly-Si films 2, 3, and 4 are obtained by receystallizing an LPCVD film by projecting ultraviolet pulse laser light using XeC as a gas source upon the LPCVD film from the upper surface of the protective film. When the intensity of the laser light is adjusted to ≥ 400 mJ/cm², the principal preferred orientation of the poly-Si film becomes (111). Then, after an SiO₂ film formed as the surface protective film is removed a photoetching process is performed for forming the poly-Si films 2, 3, and 4 recrystallized by the laser light in island-like shapes, an SiO₂ film 5 for gate insulating film is deposited by the atmospheric pressure CVD method. Consequently, a thin film semiconductor device having large carrier



mobility can be obtained.

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CLAIMS

[Claim(s)]

[Claim 1] The laser annealing approach characterized by considering as the polycrystalline silicon film which has the orientation which made {111} sides the subject for this semi-conductor layer by laser radiation in the thin film semiconductor device which has the semi-conductor film formed on the insulating substrate and this substrate.

[Claim 2] The laser annealing approach characterized by considering as the polycrystalline silicon film with the orientation which made {111} sides the subject by forming the polycrystalline silicon film with a reduced pressure CVD method at the substrate temperature of 550 degrees C or less on an insulating substrate in the laser annealing approach according to claim 1, and carrying out laser radiation of this polycrystalline silicon film.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the laser annealing approach in thin film semiconductor device manufacture, especially relates to the suitable laser annealing approach for the display of an active matrix.

[0002]

[Description of the Prior Art] In recent years, the polycrystalline silicon (Polycrystalline Silicon, omitting poly-Si) which is the point of high-definition-izing as a thin film transistor (Thin Film Transistor, omitting TFT) ingredient which is a thin film semiconductor device for active matrices, and is excellent is used. This Poly-Si film is created by the reduced pressure CVD method (LPCVD law) and the ordinary pressure CVD method (APCVD law). As an insulating substrate, quartz glass or the usual glass plate is used. Since there is big constraint of about 640 degrees C in a maximum temperature in case the usual glass plate is used, the method of recrystallizing by not having thermal effect on a glass plate, but carrying out laser radiation only of the surface layer of the Poly-Si film is tried. According to this approach, crystallinity is improving compared with low warm temperature annealing which does not affect a glass plate.

[0003] The method of irradiating an ultraviolet radiation pulse laser with a big absorption coefficient by Si film like a publication as this laser radiation approach conventionally at JP,60-245124,A, and manufacturing a semiconductor device was examined.

[0004]

[Problem(s) to be Solved by the Invention] With the above-mentioned conventional technique, the carrier mobility when the stacking tendency of the crystal of the Poly-Si film which recrystallized although the TFT property was raised by raising crystallinity by laser radiation not being examined, but creating TFT may have been raised further.

[0005] The object of this invention is to obtain still bigger carrier mobility by taking into consideration the structure of the thin film semiconductor device for raising the property of a thin film semiconductor device, and the stacking tendency of the Poly-Si film especially used for the active layer of TFT.

[0006]

[Means for Solving the Problem] It is attained by giving the orientation which made {111} sides the subject for the Poly-Si layer which constitutes TFT which is the semiconductor device formed on insulating substrates, such as a glass substrate, in the above-mentioned object.

[0007] This Poly-Si layer is 200 mJ/cm² with Si film which deposited in thickness 1500A or less in temperature with a substrate temperature of 550 degrees C or less with the reduced pressure CVD method, and was deposited below 500 degrees C. With Si film deposited at 520-550 degrees C, they are 400 mJ/cm² above. It is obtained by irradiating a laser beam from a Poly-Si layer side by the above optical reinforcement. Moreover, when Si film deposited at 550 degrees C is thin-film-ized, at

800-1500Å thickness, they are 400 mJ/cm². At 600-800Å thickness, they are 300 mJ/cm² above. At thickness 600Å or less, they are 200 mJ/cm² above. It is obtained by irradiating a laser beam from a Poly-Si layer side by the above optical reinforcement.

[0008] During Si crystal of each [film / which recrystallized by laser radiation / Poly-Si], it is few, an electronic trap is large to a grain boundary, and a defect is influenced. The phase-boundary-charge consistency of the grain boundary of Poly-Si is each crystal face of Si single crystal, and SiO₂. The same relation is materialized and the trap consistency of the film and a perpendicular direction (the <111> directions) serves as size compared with the Poly-Si film with which a stacking tendency is not seen by the Poly-Si film of {111} dominance orientation as a phase-boundary-charge consistency increases in order of <100>, <110>, and <111>. If as parallel as the film, the Poly-Si film of {111} dominance orientation will show a low trap consistency reversely relatively compared with the Poly-Si film with which a stacking tendency is not seen. The depletion-layer width of face produced on the grain community where a trap consistency is low becomes narrow, and a potential barrier here becomes low. The carrier mobility of Poly-Si is decided mainly by the height of the potential failure in a grain boundary. The carrier of TFT flows to the Poly-Si film and a parallel direction. By the Poly-Si film of these conditions to {111} dominance orientation, the mobility of a carrier becomes large relatively compared with Poly-Si without a stacking tendency.

[0009]

[Embodiment of the Invention] The example of this invention is explained below.

[0010] Drawing 1 shows the cross-section structure of the whole TFT which used this invention. A substrate 1 is a glass substrate with a distorted temperature of about 640 degrees C. A substrate 1 is kept at 550 degrees C, and the LPCVD film is made to deposit on condition that pressure 1 Torr by using as a raw material the mono-silane gas diluted with helium to 20%. Assembly time makes the 1500Å film deposit in 85 minutes. Next, a substrate 1 is kept at 480 degrees C, and 1000Å of surface protective coats is made to deposit in about 8 minutes by ordinary pressure CVD by using as a raw material the mono-silane gas and oxygen which were diluted with helium to 4%. The LPCVD film is recrystallized by irradiating the ultraviolet radiation pulse laser (wavelength of 308nm, 25ns of pulse width) which made XeCl the source of gas from the top face of this film, and the Poly-Si film 2, 3, and 4 is obtained. At this time, it is laser beam reinforcement 400 mJ/cm². The main orientation of the Poly-Si film turns into {111} dominance orientation by considering as the above, and the diameter of average crystal grain is about 1000Å. Next, SiO₂ used as a surface protective coat. The water solution of fluoric acid removes the film. It is SiO₂ for gate dielectric film by the ordinary pressure CVD method after letting the process of photoetching which forms the Poly-Si film which recrystallized by laser radiation in the shape of an island pass. The film 5 is made to deposit. Next, 3500Å of Poly-Si film 6 for gate electrodes is made to deposit on condition that 550 degrees C and 1 Torr. A phot and after sleeping together, IMPURA of the source and the drain fields 3 and 4 is performed for the gate film 5. Conditions are the dose of 5x10¹⁵cm⁻², and the electrical potential difference of 30KeV using Lynn (P). 5000Å of passivation film 8 which consists of phosphorus glass is made to deposit at 480 degrees C, and it is N₂ further. They are heat treatment of 20 hours or more, or 200 mJ/cm² at 600-degree C conditions inside. An in plastic field is activated by irradiating an ultraviolet radiation pulse laser by the above optical reinforcement. TFT is formed by carrying out 6000Å sputter of the aluminum electrode 7 the phot for contact, and after a dirty stroke.

[0011] With a reduced pressure CVD method, drawing 2 makes substrate temperature 550 degrees C, deposits 1500Å of Poly-Si, and is optical reinforcement from the Poly-Si side 100 - 400 mJ/cm². It is made to change in between and change of the X diffraction reinforcement from each field at the time of irradiating an ultraviolet radiation pulse laser and making it recrystallize and the mobility of TFT created by the above-mentioned approach is shown. Although Si (111) diffraction peak with the strongest diffraction reinforcement is increasing in proportion to optical reinforcement above threshold energy (about 100 mJ/cm²), other Si (220) and Si (311) diffraction peak are optical on-the-strength 300

20 mJ/cm². Augend becomes blunt above and a stacking tendency serves as {111} dominance orientation. 300 mJ/cm² used as {111} dominance orientation Mobility is increasing rapidly by the above optical reinforcement.

[0012] Next, the crystal stacking tendency of the Poly-Si film which irradiated the ultraviolet radiation pulse laser and recrystallized the surface protective coat deposition and after that like the backward above-mentioned publication which made deposition temperature at the time of depositing in which it is based on a reduced pressure CVD method 500-600 degrees C, and deposited the LPCVD film on drawing 3 is shown. In the LPCVD film deposited at the substrate temperature of 500 degrees C, they are 200 mJ/cm². With Si film deposited at 520-550 degrees C, they are 400 mJ/cm² above. {111} dominance orientation is not seen by Si film which became {111} dominance orientation by irradiating a laser beam by the above optical reinforcement, and was deposited at the substrate temperature of 580 degrees C or more.

[0013] Next, the crystal stacking tendency of the Poly-Si film which irradiated the ultraviolet radiation pulse laser to the backward above-mentioned publication which made substrate temperature at the time of depositing on drawing 4 with a reduced pressure CVD method 550 degrees C, shortened assembly time, and deposited the LPCVD film in 400-1500A thickness deposition and after that, and recrystallized the surface protective coat similarly is shown. In 1500A of thickness, they are 400 mJ/cm². At 800A, they are 300 mJ/cm² above. At 600A and 400A, they are 200 mJ/cm² above. It becomes {111} dominance orientation by irradiating a laser beam by the above optical reinforcement.

[0014] The electrical property which the Poly-Si film which makes the main orientation {111} stated by this example has large mobility, is using this for the active region of TFT, and was excellent can be acquired. According to the above, even if the deposition conditions of the LPCVD film differ, the Poly-Si film of {111} dominance orientation is obtained by optimizing the optical reinforcement of exposure ultraviolet radiation pulse laser light.

[0015]

[Effect of the Invention] According to this invention, a thin film semiconductor device with the large mobility of a carrier can be obtained.

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(71) 出願人 000005108
株式会社日立製作所
東京都千代田区神田駿河台四丁目6番地
(72) 発明者 小池 義彦
茨城県日立市久慈町4026番地 株式会社日立製作所日立研究所内
(72) 発明者 胡 中行
茨城県日立市久慈町4026番地 株式会社日立製作所日立研究所内
(72) 発明者 青山 隆
茨城県日立市久慈町4026番地 株式会社日立製作所日立研究所内
(74) 代理人 弁理士 小川 勝男

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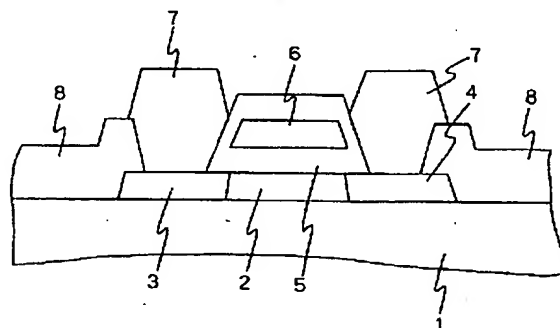
(54) 【発明の名称】 レーザアニール方法

(57) 【要約】

【課題】 キャリアの移動度が大きい薄膜半導体装置を提供する。

【解決手段】 絶縁基板上の半導体膜を、レーザアニールを用いることで{111}配向とする。

図 1



【特許請求の範囲】

【請求項1】絶縁基板と該基板上に形成された半導体膜を有する薄膜半導体装置において、レーザ照射により該半導体膜を〈111〉面を主体とした配向を持つ多結晶シリコン膜とすることを特徴とするレーザアニール方法。

【請求項2】請求項1記載のレーザアニール方法において絶縁基板上に550℃以下の基板温度で減圧CVD法により多結晶シリコン膜を形成し、該多結晶シリコン膜をレーザ照射することで〈111〉面を主体とした配向を持つ多結晶シリコン膜とすることを特徴とするレーザアニール方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は薄膜半導体装置製造におけるレーザアニール方法に係り、特にアクティブマトリクス方式のディスプレイに好適なレーザアニール方法に関する。

【0002】

【従来の技術】近年、アクティブマトリクス用の薄膜半導体装置である薄膜トランジスタ(Thin Film Transistor、略してTFT)材料としては高画質化の点ですぐれている多結晶シリコン(Polycrystalline Silicon、略してpoly-Si)が用いられている。このPoly-Si膜は減圧CVD法(LPCVD法)及び常圧CVD法(APCVD法)により作成されている。絶縁基板としては石英ガラス又は通常のガラス板を用いる。通常のガラス板を用いる際は最高温度が約640℃という大きな制約があるためガラス板には熱的影響を与えずPoly-Si膜の表面層だけをレーザ照射することで再結晶化する方法が試みられている。この方法によればガラス板に影響を与えない低温熱アニールに比べ結晶性が向上している。

【0003】従来はこのレーザ照射方法として特開昭60-245124号に記載のようにSi膜で吸収率の大きな紫外光パルスレーザを照射して半導体装置を製造する方法が検討されていた。

【0004】

【発明が解決しようとする課題】上記従来技術ではレーザ照射によって結晶性を向上させることでTFT特性を向上させていたが再結晶化したPoly-Si膜の結晶の配向性については検討されておらずTFTを作成したときのキャリア移動度を更に向上させる可能性があった。

【0005】本発明の目的は薄膜半導体装置の特性を向上させるための薄膜半導体装置の構造、とりわけTFTの能動層に使用されるPoly-Si膜の配向性を考慮することで更に大きなキャリア移動度を得ることにある。

【0006】

【課題を解決するための手段】上記目的をガラス基板等の絶縁性基板上に形成された半導体装置であるTFTを構成するPoly-Si層を〈111〉面を主体とした配向

を持たせることにより達成される。

【0007】このPoly-Si層は減圧CVD法により基板温度550℃以下の温度において1500Å以下の膜厚で堆積し、500℃以下で堆積したSi膜では200mJ/cm²以上、520～550℃で堆積したSi膜では400mJ/cm²以上の光強度でレーザ光をPoly-Si層側から照射することで得られる。又、550℃で堆積したSi膜を薄膜化した場合、800～1500Åの膜厚では400mJ/cm²以上、600～800Åの膜厚では300mJ/cm²以上、600Å以下の膜厚では200mJ/cm²以上の光強度でレーザ光をPoly-Si層側から照射することで得られる。

【0008】レーザ照射によって再結晶化したPoly-Si膜は個々のSi結晶中には欠陥が少なく電子のトラップは粒界に大きく影響される。Poly-Siの結晶粒界の界面電荷密度は、Si単結晶の各結晶面とSiO₂との界面電荷密度が〈100〉、〈110〉、〈111〉の順に増加することと同様の関係が成立し、〈111〉優位配向のPoly-Si膜では配向性の見られないPoly-Si膜に比べ膜と垂直方向(〈111〉方向)のトラップ密度が大となる。膜と平行方向では反対に〈111〉優位配向のPoly-Si膜が配向性の見られないPoly-Si膜に比べ相対的に低いトラップ密度を示すことになる。トラップ密度が低いと粒界に生じる空乏層幅はせまくなり、ここでのポテンシャル障壁は低くなる。Poly-Siのキャリア移動度は主として粒界におけるポテンシャル障壁の高さで決まる。TFTのキャリアはPoly-Si膜と平行方向に流れる。これらの条件から〈111〉優位配向のPoly-Si膜では配向性のないPoly-Siに比べ相対的にキャリアの移動度が大きくなる。

【0009】

【発明の実施の形態】以下本発明の実施例を説明する。

【0010】図1は本発明を用いたTFT全体の断面構造を示す。基板1は至温度約640℃のガラス基板である。基板1を550℃に保ち、ヘリウムで20%に希釈したモノシランガスを原料として圧力1Torrの条件でLPCVD膜を堆積させる。堆積時間は85分間で1500Åの膜を堆積させる。次に基板1を480℃に保ち、ヘリウムで4%に希釈したモノシランガスと酸素を原料として常圧CVDにより表面保護膜を約8分間で1000Å堆積させる。この膜の上面からXeClをガス源とした紫外光パルスレーザ(波長308nm、パルス幅25ns)を照射することでLPCVD膜を再結晶化しPoly-Si膜2、3、4を得る。この時レーザ光強度を400mJ/cm²以上とすることでPoly-Si膜の主たる配向は〈111〉優位配向となり平均結晶粒径は約1000Åである。次に表面保護膜として用いたSiO₂膜をフッ酸の水溶液で除去する。レーザ照射により再結晶化したPoly-Si膜を島状に形成するホトエッチングの工程を通した後、常圧CVD法によりゲート絶縁膜用の

SiO₂膜5を堆積させる。次にゲート電極用のPoly-Si膜6を550℃、1Torrの条件で3500Å堆積させる。ゲート膜5をホト、エッチした後、ソース、ドレイン領域3、4のインプラを行う。条件はリン(P)を用い、 $5 \times 10^{15} \text{cm}^{-2}$ のドーザ量、30KeVの電圧である。リンガラスからなるパッシベーション膜8を480℃で5000Å堆積させ、さらにN₂中600℃の条件で20時間以上の熱処理、あるいは200mJ/cm²以上の光強度で紫外光パルスレーザを照射することでインプラ領域を活性化させる。コンタクト用のホト、エッチ行程の後、Al電極7を6000ÅスパッタすることでTFTを形成する。

【0011】図2はPoly-Siを減圧CVD法により基板温度を550℃として1500Å堆積し、そのPoly-Si側から光強度を100～400mJ/cm²の間で変化させ紫外光パルスレーザを照射して再結晶化させた際の各面からのX線回折強度と、上記方法で作成したTFTの移動度の変化を示す。最も回折強度の強いSi(111)回折ピークはしきいエネルギー(約100mJ/cm²)以上で光強度に比例して増加しているが他のSi(220)、Si(311)回折ピークは光強度300mJ/cm²以上で増加量が鈍り配向性が{111}優位配向となる。{111}優位配向となる300mJ/cm²以上の光強度で移動度は急激に増大している。

【0012】次に図3に減圧CVD法による堆積する際の堆積温度を500～600℃としてLPCVD膜を堆積した後上記記載と同様に表面保護膜を堆積、その後紫外光パルスレーザを照射し再結晶化したPoly-Si膜の結晶配向性を示す。基板温度500℃で堆積したLPCVD膜には200mJ/cm²以上、520～550℃で堆積したSi膜では400mJ/cm²以上の光強度でレ

ーザ光を照射することで{111}優位配向となり、基板温度580℃以上で堆積したSi膜では{111}優位配向は見られない。

【0013】次に図4に減圧CVD法により堆積する際の基板温度を550℃として堆積時間を短くしてLPCVD膜を400～1500Åの膜厚で堆積した後上記記載と同様に表面保護膜を堆積、その後紫外光パルスレーザを照射し再結晶化したPoly-Si膜の結晶配向性を示す。膜厚1500Åでは400mJ/cm²以上、800Åでは300mJ/cm²以上、600Å及び400Åでは200mJ/cm²以上の光強度でレーザ光を照射することで{111}優位配向となる。

【0014】本実施例で述べた{111}を主配向とするPoly-Si膜は移動度が大きく、これをTFTの能動領域に用いることですぐれた電気特性を得ることができる。以上によれば、LPCVD膜の堆積条件が異なっても照射紫外光パルスレーザ光の光強度を最適化することで{111}優位配向のPoly-Si膜が得られる。

【0015】

【発明の効果】本発明によれば、キャリアの移動度が大きい薄膜半導体装置を得ることができる。

【図面の簡単な説明】

【図1】本発明のTFTの構造の模式図。

【図2】レーザアニール後のPoly-Siの結晶性及び移動度の光強度依存性を示す図。

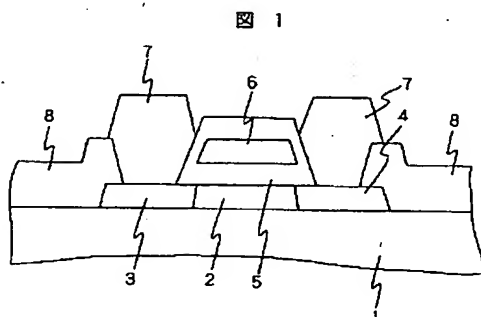
【図3】Poly-Si膜の結晶配向性を示す図。

【図4】Poly-Si膜の結晶配向性を示す図。

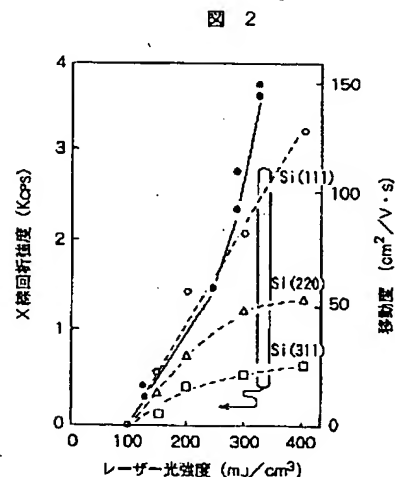
【符号の説明】

1…絶縁性基板、2…多結晶シリコン層、3…ソース領域、4…ドレイン領域、5…ゲート絶縁膜、6…ゲート電極、7…Al電極、8…パッシベーション膜。

【図1】



【図2】



【図3】

成膜温度 (°C) 光強度 (mJ/cm ²)	500	520, 550	580, 600
0	アモルファス	アモルファス	{110} 優位配向
200	{111} 優位配向	配向性なし	{110} 優位配向
300	{111} 優位配向	配向性なし	配向性なし
400	{111} 優位配向	{111} 優位配向	配向性なし

図
3

【図4】

成膜温度 (°C) 光強度 (mJ/cm ²)	400	600	800	1500
0	アモルファス	アモルファス	アモルファス	アモルファス
200	{111} 優位配向	{111} 優位配向	配向性なし	配向性なし
300	{111} 優位配向	{111} 優位配向	{111} 優位配向	配向性なし
400	{111} 優位配向	{111} 優位配向	{111} 優位配向	{111} 優位配向

図
4

フロントページの続き

(72)発明者 岡島 義昭

茨城県日立市久慈町4026番地 株式会社日立

立製作所日立研究所内